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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/783,771	BIGBEE ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-10,12-15,17-19 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-10,12-15,17-19 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 12-18 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 3-9 respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, line 1, it is not clear what is meant by "the method of claim 3" since claim 3 is not a method claim. Similar

problems exist in claims 5-9 since claim 3, the independent claim, is not a method claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-6, 10, 12-15, 19, 21, and 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Juffa (U.S. Patent No. 6,247,117) (hereafter referred to as Juffa'117).

Referring to claim 1, Juffa'117 discloses, as claimed, a method comprising: writing an initial value (CF value before it is replaced by DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) to at least one address within a memory image (262, Architectural Flags Register, see Fig. 6B) residing in dynamic random access memory (note the Architectural Flags Register 262

inside the Flags Register 230 are best reasonably and broadly interpreted as a dynamic random access memory since it can be dynamically and randomly accessed), said memory image being generated as a result of performing a state save operation (such as the operations by executing instructions FCOMI, FCOMIP, FUCOM, and FUCOMIP, see Col. 19, lines 56-60, regarding setting (or generating) the one or more flags of architectural flags registers.); adjusting a control value for a control register (262, Flags register, see Fig. 6B) as a function of said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) to generate a masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9); storing (through the numerous checking instruction to set a flag, see Col. 21, lines 11-14) said masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9) into the control register (262, Flags register, see Fig. 6B).

Referring to claim 10, Juffa'117 discloses, as claimed, a machine-readable medium (in the maim memory or instruction cache 16, see Fig. 3) having stored thereon a set of instructions said set of instructions, which when executed by a processor, cause said processor to perform a method comprising: writing an initial value (CF value before it is replaced by DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) to at least one address

within a memory image (262, Flags register, see Fig. 6B) residing in dynamic random access memory (note the Architectural Flags Register 262 inside the Flags Register 230 are best reasonably and broadly interpreted as a dynamic random access memory since it can be dynamically and randomly accessed); said memory image being generated as a result of performing a state save operation (such as the operations by executing instructions FCOMI, FCOMIP, FUCOM, and FUCOMIP, see Col. 19, lines 56-60, regarding setting (or generating) the one or more flags of architectural flags registers); adjusting a control value for a control register (262, Flags register, see Fig. 6B) as a function of said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A)to generate a masked control value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9); storing (through the numerous checking instruction, see Col. 21, lines 11-14) said masked control value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) into the control register (262, Flags register, see Fig. 6B).

Referring to claim 19, Juffa'117 discloses, as claimed, an apparatus comprising: a control register (262, Flags register, see Fig. 6B) comprising a plurality of bits (such as CF, PF, and ZF bits in Fig. 6B) corresponding to a plurality of functions (note such as: CF is for carry flag; PF is for parity flag; and

ZF is for zero flag. Each one provides a specific function, see also Col. 19, lines 25-33); a masking mechanism (the mechanism inherently existing in the Juffa'117's system for setting such as CF, PF, and ZF values in Fig. 9) to generate a control register mask by setting inactive one or more bits (see Fig. 9, last column, CF, PF, and ZF are set inactive by "0") of a control value prior to storage of said one or more bits in the control register (see such as 2nd column in Fig. 9), wherein the masking mechanism (the mechanism certainly existing in the Juffa'117's system for setting such as CF, PF, and ZF values in Fig. 9) includes a mask storage area (control register 270, see Fig. 7A) within dynamic random access memory (note control register 270, see Fig. 7A, is best reasonably and broadly interpreted as a dynamic random access memory since it can be dynamically and randomly accessed) to store state information (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A) corresponding to state information stored in the control register, said mask storage area having been generated as a result of performing a state save operation (similar to the operations by executing instructions FCOMI, FCOMIP, FUCOM, or FUCOMIP, see Col. 19, lines 56-60, regarding signaling register file 30 to set (or generate) the one or more flags of architectural flags registers, the control register 270 (interpreted as mask storage area) certainly

must be set or generated during the state save operations in the Juffa'117's system).

As to claims 3 and 12, Juffa'117 also discloses: further comprises executing a state save operation (as set forth in claim 10, such as the operations by executing instructions FCOMI, FCOMIP, FUCOM, and FUCOMIP, see Col. 19, lines 56-60, regarding setting (or generating) the one or more flags of architectural flags registers).

As to claims 4 and 13, Juffa'117 also discloses: further comprises comparing a saved value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) to said initial value (CF value before it is replaced by the DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9), said saved value (DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) being stored within said memory image as a result of said execution of said state save operation (as set forth, inherent step in the Juffa'117's system).

As to claims 5 and 14, Juffa'117 also discloses: said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) is set to a default value ("0" , see Fig. 9) if said saved value is equal to said initial value ("0" , see last column in Fig. 9).

As to claims 6 and 15, Juffa'117 also discloses: said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) being set to said saved value if said saved value is not equal to said initial value (note CF value is replaced by the DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9).

As to claims 21, Juffa'117 also discloses: said mask storage area (control register 270, see Fig. 7A) may be accessed by performing a state saving operation which saves said mask value (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A) to a memory location (see Fig. 9, DM is stored in 7th column).

As to claims 23, Juffa'117 also discloses: said masking mechanism is a hardware masking mechanism (the hardware mechanism certainly existing in the Juffa'117's system for setting such as CF, PF, and ZF values in Fig. 9).

As to claims 24, Juffa'117 also discloses: said masking mechanism comprises: a sequence of instruction (saved in the main memory or cache memory of the processor 10, see Fig. 3) to adjust a control value by saving state Information including a control register value to a memory and adjusting said control register value based on a readable mask value read from the processor before restoring the state information; execution hardware to

execute the sequence of instructions (see described as set forth in claim 1 above).

Referring to claim 25, Juffa'117 discloses, as claimed, a processor (processor 10, see Fig. 3) comprising: a decode unit (such as decode unit 24A, or 20B, or 20C, see Fig. 3); at least one of a plurality of registers (such as 270, control Register, see Fig. 7A, in register file 30, se Fig. 3, see also Column 20, line 6-7), said at least one of a plurality of registers comprising a plurality of bits (such as IM, DM, ZM, OM, UM, and PM bits in Fig. 7A) corresponding to a plurality of functions (note IM, DM, ZM, OM, UM, and PM bits in Fig. 7A each one provides a specific function, see also Col. 19, lines 65 to Column 20, lines 1-7); a masking mechanism (the mechanism inherently existing in the Juffa'117's system for setting such as CF, PF, and ZF values in Fig. 9) to generate a control register mask by setting inactive one or more bits (see Fig. 9, last column, CF, PF, and ZF are set inactive by "0") of a control value prior to storage of said one or more bits in the control register (see such as 2nd column in Fig. 9), wherein the masking mechanism includes a mask storage area (control register 270, see Fig. 7A) within dynamic random access memory (note control register 270, see Fig. 7A, is best reasonably and broadly interpreted as a dynamic random access memory since it can be

dynamically and randomly accessed) to store state information (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A) corresponding to state information stored in the at least one of the plurality of register, said mask storage area having been generated as a result of performing an instruction (similar to the instructions FCOMI, FCOMIP, FUCOM, or FUCOMIP, see Col. 19, lines 56-60, regarding signaling register file 30 to set (or generate) the one or more flags of architectural flags registers, the control register 270 (interpreted as mask storage area) certainly must be set or generated during the state save operations in the Juffa'117's system); an execution unit (such as Function units 24A, 24B, and 24C); an internal bus (38, see Fig. 3), said decoder unit (such as decode unit 24A, or 20B, or 20C, see Fig. 3, said at least one plurality of registers (such as 270, control Register, see Fig. 7A, in register file 30, se Fig. 3, see also Column 20, line 6-7), said at least one execution unit (such as Function units 24A, 24B, and 24C being coupled by said internal bus (38, see Fig. 3).

As to claims 26, Juffa'117 also discloses: in response to said execution unit (such as Function units 24A, 24B, and 24C) executing an instruction, said plurality of bits (such as DM value under such as FSCALCHK, and FSIINCHK, see Fig. 9) are

written to the mask storage area (262, Flags register, see Fig. 6B and see DM and IM in Fig. 9).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8, 9, 17, 18, 22, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juffa (U.S. Patent No. 6,247,117) (hereafter referred to as Juffa'117).

Juffa'117 discloses the claimed invention except for: explicitly defining the state saving operation is an FXSAVE instruction (claims 8, 17, 22 and 27); the at least one of a plurality of registers is an MXCSR register (claim 28); and the mask storage area is an MXCSR MASK field (claim 29).

However, FXSAVE is just an instruction name and MXCSR and MXCSR MASK field are just a register and field name. Juffa'117's

system certainly provides the same features as the FXSAVE instruction and MXCSR register and MXCSR MASK field.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Juffa'117's system to comprise: the state save operation is an FXSAVE instruction, and the FXSAVE instruction having an associated target address; said at least one of a plurality of registers is an MXCSR register; and the mask storage area is an MXCSR MASK field since they are just an alternative name comparing with that used by the Juffa'117's system.

Note as to claims 9 and 18, a save instruction having an associated target address is certainly existing in a save operation for a saved destination in the Juffa'117's system.

As to claims 9 and 18, Juffa'117 also discloses: the target address being an address within the memory image (262, Architectural Flags Register, see Fig. 6B).

Response to Amendment

8. Applicant's arguments filed 7/25/05 have been fully considered but they are not deemed to be persuasive.

Regarding the 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these objections and rejections.

Applicants argue that "Juffa, on the other hand, does not teach a memory image or mask storage area as claimed by applicant nor a memory image or mask storage area that is generated by the performance of a save state operation or any other operation or instruction, as claimed by Applicant in presently amended claims 1, 10, 19, and 25." (page 9, lines 15-19). Examiner disagrees with Applicants. As set forth in the art rejections above, Juffa'117 discloses: a memory image (262, Architectural Flags Register, see Fig. 6B) residing in dynamic random access memory (note the Architectural Flags Register 262 inside the Flags Register 230 are best reasonably and broadly interpreted as a dynamic random access memory since it can be dynamically and randomly accessed), said memory image being generated as a result of performing a state save operation (such as the operations by executing instructions FCOMI, FCOMIP, FUCOM, and FUCOMIP, see Col. 19, lines 56-60, regarding setting (or generating) the one

or more flags of architectural flags registers.); adjusting a control value for a control register (262, Flags register, see Fig. 6B) as a function of said control register mask (such as DM (denormal maskbit) in control register 270, see Fig. 7A) to generate a masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9); storing (through the numerous checking instruction to set a flag, see Col. 21, lines 11-14) said masked control value (DM value for CF under such as FSCALCHK, and FSIINCHK, see Fig. 9) into the control register (262, Flags register, see Fig. 6B).

Juffa'117 also discloses: a mask storage area (control register 270, see Fig. 7A) within dynamic random access memory (note control register 270, see Fig. 7A, is best reasonably and broadly interpreted as a dynamic random access memory since it can be dynamically and randomly accessed) to store state information (such as IM, DM (denormal maskbit), ZM, OM, UM, or PM see Fig. 7A) corresponding to state information stored in the control register, said mask storage area having been generated as a result of performing a state save operation (similar to the operations by executing instructions FCOMI, FCOMIP, FUCOM, or FUCOMIP, see Col. 19, lines 56-60, regarding signaling register file 30 to set (or generate) the one or more flags of architectural flags registers, the control register 270

(interpreted as mask storage area) certainly must be set or generated during the state save operations in the Juffa'117's system).

In summary, Juffa'117 teaches the claimed invention.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

September 27, 2005